Designing PCBs For Test And Inspection

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End-product costs can rise considerably when engineering changes are made late in a printed circuit board's (PCB's) design and development cycle. Up to 80% of a new product's cost is often committed by the first prototype build. This article provides practical and affordable Design-for-Test (DFT) and Design-for-Inspection (DFI) methods that will have a positive impact on product costs, yield, reliability, and time-to-market. The properties of testability (including controllability and observability) will be analysed as they relate to analogue and digital design rules and their cause/effect, as well as the electrical and physical characteristics of proper PCB design.

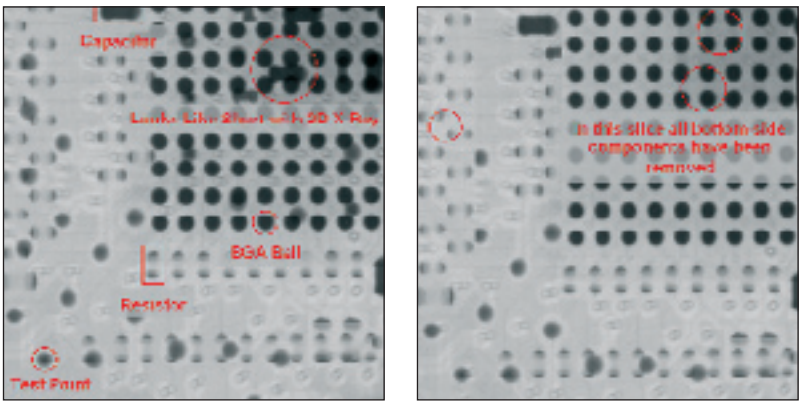


Figure 1 - Boards are becoming more complex

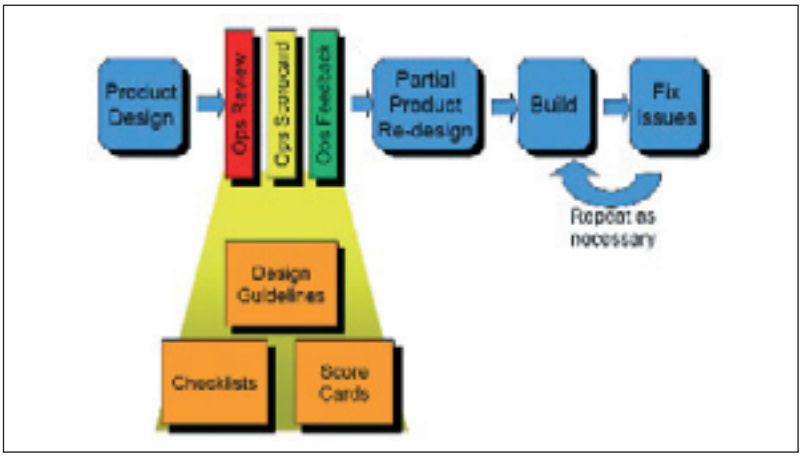


Figure 2 - DFI/DFT workflow

Increasing test and inspection challenges

A number of different PCB trends have converged and increased the challenge of improving test and inspection methods. The most obvious trend is the movement towards new chip packages and board assembly technologies, and increasing component and pad densities that reduce electrical and optical access to PCBs. The average density on wireless devices is already approaching 50 I/Os per square inch, a point at which in-circuit testing becomes more difficult and requires new techniques. Higher speeds and lower voltages can also restrict electrical access because ICT signal integrity and accuracy tend to become much more challenging above 500 MHz as testpoints can affect the performance of the design.

Optical inspection has its own unique set of problems. Automated optical inspection (AOI) is increasingly challenged by the growing use of technologies that restrict visual access. These include component technologies with hidden joints such as ball grid array (BGA), flip-chips, fine pitch, and small pad 0201s. Mechanical fixtures such as RF shields can also restrict visual access to components and joints. Technologies that present problems for visual inspection are growing at a rapid rate, with the percentage of joints that cannot be inspected by AOI systems projected to increase to nearly 50% by 2007.

Even automated x-ray inspection (AXI), which potentially offers the ability to overcome many of these challenges because it does not require either visual or electrical access, is experiencing some challenges in the new environment. One concern is that Lead-free solder is typically about 20% less dense than conventional solder. This often requires test programs to be recalibrated in order to distinguish solder from background material and may require an increase in the number of grey levels detected by the x-ray system to provide better resolution.

Conventional product development methods

In conventional product development methods, test and inspection challenges are not considered in detail until the product design process is completed and the design is thrown "over the wall" to manufacturing. Manufacturing is then responsible for building a prototype and evaluating manufacturing, test, and inspec-

tion methodologies. Not surprisingly, the initial design will more often fail to meet manufacturability, testing, and inspection requirements because these requirements were not addressed during the design process.

The design may be changed several times during the prototype build stage to accommodate manufacturing, test and inspection issues. This is expensive because the large amount of resources that are invested at each stage of the product development cycle typically increases the cost of an equivalent change by a factor of 10 at each successive stage. For example, it costs approximately 10 times as much to make a change in the detailed product design stage compared to the concept design stage, 10 times as much in prototype build as in detailed product design; and 10 times as much in production as in prototype build. These numbers are very rough approximations, of course, but it's hard to ignore the basic principle that substantial time and cost savings can be achieved by identifying problems and optimising the performance of manufacturing, inspection and test as early as possible.

Benefits of DFI and DFT

While Design-for-Manufacturability (DFM) has been an area of focus for some time now, electronics manufacturers are increasingly recognising the importance of increased attention to DFI and DFT. DFI and DFT are a class of design methods intended to place constraints on the design process in order to make test design and execution more comprehensive and less expensive, thus optimising test-related production costs.

Many manufacturers who have embarked on this process have discovered that design changes made to improve one of these areas can adversely affect other areas. As a result, a new integrated methodology is emerging, called Design-for-X (DFx) or Design-for-eXcellence. The goal of DFx is to develop design methodologies, techniques, and work practices that enable a product to be designed and manufactured at the lowest possible manufacturing cost, highest quality, and optimal lifecycle support while taking manufacturing, inspection, and test into account.

At the heart of DFI and DFT is the development of a set of design guidelines and methodologies that help ensure the success of inspection and test operations on the specific products and test and inspection methods used by a particular manufacturer. Generally, the guidelines are used to develop checklists used during the design process to evaluate alternative design concepts. The concepts are compared against the checklists to produce a scorecard for evaluating each concept against the goal of optimising all of the factors considered important in the success of the product.

While this approach (often driven by necessity) lengthens the amount of time required for concept design, it can substantially reduce the costs and leadtime involved in downstream operations including detailed product design, prototype build and production. This is because problems are identified and processes are optimised at a much earlier stage. DFI and DFT also have the benefit of generating measurable metrics on design factors that affect inspection and test operations. These metrics can be evaluated against important results such as product cost, reliability, and yield with the goal of improving the outcomes on future development projects.

Physical rules

The rules used for DFI and DFT are generally divided into two categories - physical and electrical. Physical rules largely focus on the characteristics of the boards themselves in order to ease both tactile and optical access to components and joints. For example, both AOI and AXI use conveyors that grip PCBs by their edges to position them for inspection. This means that at least 3.18 mm (0.125 inch) of the board must be free of components and traces to provide room for grippers to properly operate.

For in-circuit testing (ICT), the greatest concern is typically the clearance on the bottom of board. The type of fixture and probes used generally limits the height of components on the bottom to less than 3.81 mm (0.150 inches) for standard fixtures. Special fixtures can provide clearance of up to 76 mm (3 inches). ICT also generally provides side clearance of 3.18 mm (0.125 inch). For AOI, which operates on one side of the board only, clearance on the top of the board is generally the primary concern, where limitations between 25 mm (1 inch) and 50 mm (2 inches) are typical. AXI systems, because they require both an x-ray source and a detector, typically provide between 25 mm (1 inch)

Figure 3 - Allowable density of standard 113 gram (4 oz.) probes vs. board thickness

Thickness	<34 probes per inch^2	35 to 64 probes per inch^2	65 to 128 probes per inch^2	129 to 196 probes per inch^2
.050 inch	Yes	No	No	No
.065 inch	Yes	Rule B	No	No
.100 inch	Yes	Rule A	Rule B	Rule C
.125 inch	Yes	Yes	Rule A	Rule D

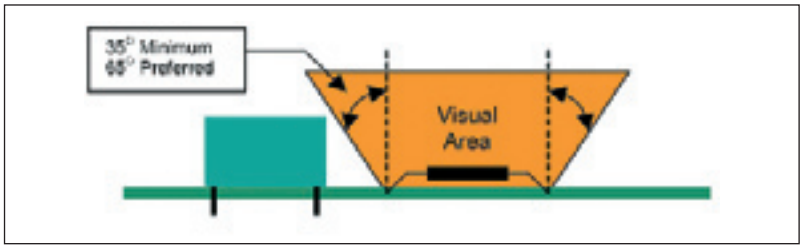


Figure 4 - Visual area is important for optical test

and 38 mm (1.5 inches) of clearance on both sides of the PCB.

ICT provides some additional special requirements. Three tooling holes (at least two of which are diagonally opposed to each other) are preferred because locating holes on both ends of the board increases positioning accuracy. These holes should be positioned within 0.05 mm (0.002 inch) of each other, have a diameter of 3.25 mm (0.128 inch), be more than 3.18 mm (0.125 inch) from the edge, not be obscured by components, and not be plated so they do not pick up solder. Test points should all reside on a single side of the board, be distributed as evenly as possible, provide a minimum of one test point per Net, and be positioned as close as possible to the signal source.

Test pads should have a bottom side diameter greater than 7.1 mm (0.28 inch) and a topside diameter greater than 8.1 mm (0.32 inch). They should be square in order to provide a 27.5% larger target than a round pad. Pad size should be within +/-0.05 mm (0.002 inch) and pad-to-pad accuracy within +/-0.05 mm (0.002 inch). Centre-to-centre test pad spacing of 2.2 mm (0.085 inch) or greater is preferred because it allows the use of 100 mil technology probes. Test-pad spacing of between 1.8 mm (0.070 inch) to 2.2 mm (0.085 inch) is acceptable because it allows use of 1.9 mm (75 mil) technology probes. Test pads should be at least 5 mm (0.200 inch) from the tooling pin, and it is preferable to have at least a 1.3 mm (0.050 inch) spacing from the edge of a test pad to the closest point on a component.

Optical access is a major consideration whenever AOI is to be used. Maintaining consistent board colour can be a concern because significant changes in board colour may make it more difficult to pick out objects such as components and solder beads from the background. It is also important to ensure that components are marked consistently, with characters of the same size and type and in the same position. The viewing area, which is the largest angle from the perpendicular by which the component or joint can be viewed, is critical so that components can be detected in other than a head-on camera position. While 35° is usually considered to be the minimum viewing angle, 65° is better. Finally, specific levels of separation need to be maintained between components and joints so that the AOI system can distinguish between them.

Overlapping solder joints on the top and bottom of the board provide a challenge for certain types of AXI. It is still possible to inspect overlapping solder joints with 3D AXI, but this approach typically increases both test development and cycle time. Certain types of dense devices or fixings can also present challenges for AXI by obscuring components and joints. These include certain capacitor types, slugs, strengthens, heat sinks and dense RF shields. These types of components are particularly troublesome with 2D x-ray technology, while 3D AXI can more often provide angled images that make it possible to see around such obscurants.

Electrical rules

Equally important rules can be defined for electrical design for inspection and test. In analogue design, parallel resistor/inductor circuits are difficult to test, so whenever possible the resistance should be divided into two components with a test pad positioned between them. Likewise, three-pin polarised capacitors should be used whenever possible because two-pin polarised capacitors cannot easily be tested for polarity.

Turning to digital design, it is important to add a test point on the enable pin of oscillators through a resistor so that they can be turned off during ICT. This is to avoid high frequency signals and noise that may interfere with other traces. A test point should also be added to the power reset so that the device can easily be put into a defined state for ICT or functional testing. Resets can often be accomplished by other methods but a power reset is usually the fastest approach so use it whenever possible to minimise beat rate. Unused inputs should also be tied off by resistor with test pads in order to verify input integrity, avoid propagating unused faults, and fa-

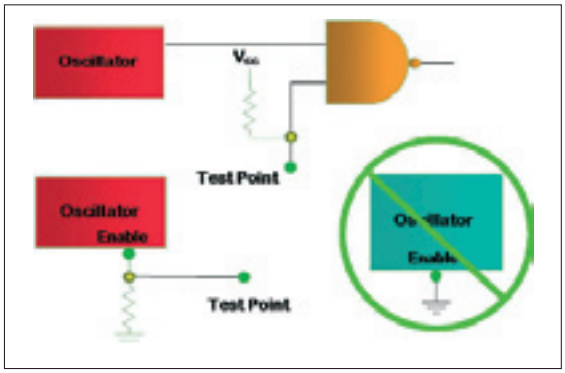
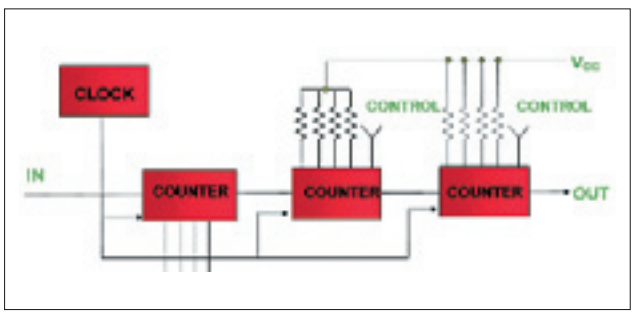


Figure 5 (left) - Controlling oscillator timing
Figure 6 (right) - Break serial chains with test pins



cilitate engineering changes. Floating inputs caused by defects can generate noise that prevents the PCB from working correctly.

It is always best to break serial chains with test pins that access the control for each component directly, especially for functional testing. This makes it possible to preload counters to minimise the number of steps involved in functional testing. Another concern is that TCLK, a test clock overdriven on the XTAL_IN input during test mode in a Pentium chip, has a specified minimum rise time. This requires a buffer in order to avoid a double rise. When programming flash EEPROM, it is important to avoid the situation where inspection stimulates and reprograms the device. As a rule, when testing flash EEPROM, don't program the protection bit until after testing and don't use hardware fault insertion.

Boundary-scan testing presents special challenges for DFT. All points in the test access port (TAP) must have test points. TAP inputs must be properly terminated unless this is done internally with a pull up/down resistor. A typical resistor value is 1 KΩ. All device outputs must be tri-stateable. If IEEE 1149.1 compliant, the JTAG signal TDO is the only output pin that should remain active when the tri-state pin is enabled. Some systems require only one boundary-scan chain. If the boundary-scan is not IEEE 1149.1 compliant, a pass-through mode can be designed into the device that allows signals to pass directly from input pins to outputs in only a couple of states. Another approach is to use dual height fixturing, which means that all probes are connected during in-circuit tests (fewer during functional tests) to reduce the loading effects of probes and wiring.

Power distribution is an important issue to consider, particularly for boundary-scan. A situation where all outputs change at the same time could cause ground bounce, so it is important to provide as many ground traces as possible, provide a solid ground plane under the board, and connect multiple ground planes to the tester with Copper braid. Be wary of situations where the test point may influence the circuit. In particular, high frequency signals above 500 to 600 MHz are affected by discontinuities, so they may require buffers or the use of capacitive probes. A particularly sensitive circuit may need to be tested functionally or as a cluster.

Future challenges

It is also important to anticipate changes in DFT and DFI strategies and adapt to changing technologies. Expect increases in PCB node densities, improvements in boundary-scan technology, and migration to Lead-free technologies to continue. In response, ICT fixtures will improve. For example, the latest fine-point alignment methods make it possible to position the probe with 0.12 mm (0.005 inch) accuracy. New fine-point probing assemblies can enable the use of probes, tight spacing and local alignment using optics to align lines, tracks, and rotating location pins on boards in order to increase probing accuracy. Pads or small solder bumps/beads can be used with simple flat-headed probes or probes with conductive material.

Advancements in boundary-scan methods will also help address the testing challenges of the future. Improvements to standards include the 1149.4 standard for mixed signal test buses, the 1149.6 standard for boundary-scan testing of advanced digital networks, and the IEEE 1532 standard for in-system configuration of programmable devices. Boundary-scan is increasingly being adopted for other uses, such as in-system programming (ISP) debug.

These guidelines provide general rules for optimising test and inspection during the initial design phase. While they are generally applicable to many applications, each electronics assembler should develop specific principles that match their product mix and test and inspection strategies. This will ensure the optimisation of product designs during the initial design phase, resulting in substantial savings in time and money during product design and prototype build.